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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,175	06/24/2003	Eugene B. Hinterscher	TI-36136	9443
23494	7590 03/09/2004		EXAM	INER
TEXAS INSTRUMENTS INCORPORATED			NGUYEN, LONG T	
	P O BOX 655474, M/S 3999 . DALLAS, TX 75265		ART UNIT	PAPER NUMBER
			2816	· · · · · · · · · · · · · · · · · · ·
			DATE MAILED: 03/09/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)
	10/602,175	HINTERSCHER, EUGENE B.
Office Action Summary	Examiner	Art Unit
	Long Nguyen	2816
The MAILING DATE of this commun Period for Reply	ication appears on the cover sheet wi	th the correspondence address
A SHORTENED STATUTORY PERIOD F THE MAILING DATE OF THIS COMMUN - Extensions of time may be available under the provisions after SIX (6) MONTHS from the mailing date of this comm - If the period for reply specified above is less than thirty (3 - If NO period for reply is specified above, the maximum st - Failure to reply within the set or extended period for reply Any reply received by the Office later than three months a earned patent term adjustment. See 37 CFR 1.704(b).	ICATION. s of 37 CFR 1.136(a). In no event, however, may a renunication. sto) days, a reply within the statutory minimum of third atutory period will apply and will expire SIX (6) MON will, by statute, cause the application to become AB	eply be timely filed y (30) days will be considered timely. THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).
Status		
3) Since this application is in condition	2b)⊠ This action is non-final.	•
Disposition of Claims		
4) Claim(s) 1-4 is/are pending in the ap 4a) Of the above claim(s) is/a 5) Claim(s) is/are allowed. 6) Claim(s) 1-4 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restrict Application Papers 9) The specification is objected to by the 10) The drawing(s) filed on 24 June 2003 Applicant may not request that any object Replacement drawing sheet(s) including	re withdrawn from consideration. ction and/or election requirement. e Examiner. is/are: a) accepted or b) objection to the drawing(s) be held in abeyand the correction is required if the drawing(s)	ce. See 37 CFR 1.85(a). (s) is objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim a) All b) Some * c) None of: 1. Certified copies of the priority 2. Certified copies of the priority 3. Copies of the certified copies	documents have been received. documents have been received in A of the priority documents have been nal Bureau (PCT Rule 17.2(a)).	pplication No received in this National Stage
Attachment(s)	,, □	(770.440)
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PB) Information Disclosure Statement(s) (PTO-1449 or Paper No(s)/Mail Date 6/24/03. 	TO-948) Paper No(s	ummary (PTO-413))/Mail Date formal Patent Application (PTO-152)

DETAILED ACTION

Claim Objections

1. Claims 3 and 4 are objected to because of the following informalities:

In claim 3, line 15, "a voltage" should be changed to --another voltage-- to avoid unclear antecedent basis problem since "a voltage" already recited on line 13 of the same claim.

Claim 4 is objected to because it includes the minor informalities of claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 2, the recitation "further comprising a tristate circuit adapted to cause the output node to be in a tristate condition in response to a tristate enable input signal" appears to be misdescriptive because it is inconsistent with what is disclosed and shown. As it is seen in Figure 1 of the drawings, the pre-driver (11, 12) receiving the tristate enable input signal for causing the output node to be in a tristate condition. Thus, it appears that there is no such tristate circuit (beside the damping control circuit branch, the output transistor and the predriver circuit) in the output circuit. Clarification and/or appropriate correction is requested.

With respect to claim 4, this claim is indefinite for the similar reasons as discussed in claim 2 above. Note that Figure 1 shows the upper pre-driver circuit (11) and the lower pre-

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driver circuit (12) receive the tristate enable signal (tri) for causing the output node (out) to be in a tristate condition, and there is no such tristate circuit (beside the upper damping control circuit branch, a lower damping control circuit branch, an upper output transistor, a lower output transistor, an upper predriver circuit, and a lower predriver circuit) in the output circuit. Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Bancal (USP 6,028,574).

With respect to claim 1, Figure 5 of the Bancal reference discloses an output circuit, which includes: a damping control circuit branch (D22, R5) comprising a resistor (R5) and a diode (D22) connected in parallel between a first node (junction connection of transistor M5 and diode D22 and resistor R5) and a second node (20), the second node (20) being coupled to an output node (20); an output transistor (MN) coupled by its source and drain between a power supply (ground supply M) and the second node (junction connection of transistor M5 and diode D22 and resistor R5), and having a gate (gate of MN); and a predriver circuit (R4) receiving an input signal (CN) and provide a voltage at the gate (gate of MN).

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Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ten Eyck (USP 6,137,322) in view of Lin (USP 6,552,594).

With respect to claims 1-4, Figure 1 of the Ten Eyck reference discloses an output circuit, which includes: a pull-up circuit (28) including an upper output transistor (28) connected between a power supply (38) and an output node (42); a pull-down circuit (22) including a lower output transistor (22) connected between ground (40) and the output node (42); an upper predriver circuit (23, 24, 26, 27) receiving an input signal (34) and provide a voltage at the gate of the upper output transistor (28); and a lower pre-driver circuit (20, 21, 29, 30) receiving the input signal (34) and provide another voltage at the gate of the lower output transistor (22). The Ten Eyck reference does not disclose that the pull-up circuit including an upper damping control circuit connected between the upper output transistor and the output node, and the pull-down circuit including a lower damping control circuit connected between the lower output transistor and the output node, wherein the upper damping control circuit comprising a first diode and a first resistor connected in parallel, and wherein the lower damping control circuit comprising a second diode and the second resistor connected in parallel. However, the Lin reference discloses in Figure 11A an output circuit that includes a pull-up circuit (60) and a pull-down circuit (62). wherein the pull-up circuit (60) including a resistance modulator (the diode and resistor

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connected in parallel in the pull-up circuit 60 in Figure 11A) connected between the upper output transistor (P1) and the output node (64), and the pull-down circuit (62) including another resistance modulator (66) connected between the lower output transistor (N1) and the output node (64) for the purpose of suppress the voltage ringing and overshooting (lines 12-37 of Col. 6, and lines 11-24 of Col. 7). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Ten Eyck reference by providing the output circuit in Figure 1 of the Ten Eyck reference with a first resistance modulator connected between the upper output transistor and the output node, and a second resistance modulator connected between the lower output transistor and the output node, wherein the first resistance modulator comprising a first diode and a first resistor connected in parallel, and the second resistance modulator comprising a second diode and the second resistor connected in parallel as taught in Figure 11A of the Lin reference for the purpose of voltage ringing and overshooting suppression. Thus this modification/combination meets all the limitations of claims 1-4. Note that the upper damping circuit and the lower damping circuit are the first resistance modulator and the second resistance modulator, respectively. Also note that, in Figure 1 of the Ten Eyck reference, the upper and lower pre-driver circuits receive the tristate enable signal (36) for causing the output node (42) to be in a tristate condition in response the tristate enable input signal (36).

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Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

February 26, 2004

Long Nguyen

Primary Examiner, AU 2816